REMARKS

Claims 10-30 remain in this application. Claims 1-9 are cancelled. Claims 13 and 20 are amended.

Applicant thanks the Examiner for the detailed study of the application and prior art. At the outset, the specification at paragraph 22 has been corrected and the minor claim objections to claim 20 corrected. Claim 13 has been amended to state that the priority value from the stack register corresponding to the interrupt service routine whose execution was recently serviced is cancelled.

At the outset, Applicant notes that this application is directed to a method (claims 10-19), control circuit (claims 20-24), and microprocessor system (claims 25-30) that changes the priorities of interrupts with dedicated hardware and reduces the activity of a central processing unit to ensure a fast execution of the most critical interrupt routines.

As set forth in the claims, this function can be accomplished by storing interrupts in a pending interrupts register and storing the priority values associated with the stored interrupts in a plurality of priority registers coupled to the pending interrupts register. A plurality of counters are coupled in cascade to the plurality of priority registers and loaded with stored priority values. At predetermined intervals the priority values are loaded and the counters are incremented. These priority values are compared for identifying an interrupt having a highest priority when that interrupt is processed. This is set forth in claim 14. Claim 10 indicates that this comparison can be made if a routine is not executed and the interrupt having the highest priority is

processed by generating an interrupt command and an interrupt vector identifying the interrupt service routine to be executed. The interrupt having the highest priority from the pending interrupts register and its priority value from the plurality of priority registers is cancelled.

The Examiner has initially rejected claim 10 as unpatentable over U.S. Patent No. 6,807,595 to Khan et al. (hereinafter "Khan"), in view of U.S. Patent No. 5,392,033 to Oman et al. (hereinafter "Oman"), and further in view of U.S. Patent No. 5,274,774 to Manber et al. (hereinafter "Manber"). Claims 11 and 12 are considered unpatentable over Khan in view of Aman, in view of Manber, and further in view of U.S. Patent Publication No. 2002/0181455 to Norman et al. (hereinafter "Norman"). Other claims are rejected as unpatentable over Khan in view of Oman and further in view of Manber (claims 13, 14, 15 and 19), or unpatenable over Khan in view of U.S. Patent No. 5,918,057 to Chou et al. (hereinafter "Chou"), and further in view of Oman or Khan in view of Chou in view of Oman and further in view of Norman.

This is a large number of references and Applicant contends that even the first two references cited by the Examiner, i.e., Khan and Oman, do not suggest the combination of the claimed invention.

Khan discloses a similar architecture as shown in FIG. 1 (prior art) of the instant application, in which the interrupt controller manages the interrupt priorities and interrupt vectors. It uses an interrupt controller and prioritizes the interrupt request on behalf of the microprocessor. An interface unit receives the interrupt requests from peripheral processing units. An interrupt

prioritization circuit identifies the interrupt request of highest priority through the use of a prioritization register that maintains a predetermined priority level associated with each of the individual interrupt lines. A plurality of interrupt level slice units are associated with the predetermined priority level. A received interrupt request can be based on an interrupt request line upon which the interrupt is received. The interrupt level slice units are provided at one per respective priority level, with each receiving a value representative of all interrupt requests and outputting a value representative of only those interrupt requests having the respective priority level. This system uses a round-robin selection unit for selecting one interrupt among a group of interrupts of each priority.

Thus, there is no necessity for using any type of priority counters as in the claimed invention. Khan actually negates any use of priority counters and instead teaches the use of an interrupt controller in association with the prioritization circuit and slice units.

As to Oman, it includes counters that modify interrupt priorities, but for a much different purpose. Oman is directed to the use of LAN networks and not interrupt controllers as clearly shown in FIG. 1 of Oman. The counters are added for implementing a round-robin algorithm in which channels have periodically increasing priorities and return to a minimum priority level. This allows priority to be determined for accessing a bus by a resource on a shared bus. This function is clearly set forth starting at column 13 at line 64 and continuing on through column 14 at line 30 as indicated below:

"The operation of the present invention will now be described. The priority generators 121 of the present invention can be programmed to provide a variety of priority schemes, with the minimal hardware described. The priority generators can provide fixed priority, first-come first-serve priority, round robin priority, and a combination of fixed and round robin priorities.

To provide fixed priority, the inputs I of all of the priority generators are set at different initial starting values. For example, if LAN #4 is to have the highest priority, followed by LAN #3, which is followed by LAN #2, which is followed by LAN #1, then inputs I(4) for the fourth priority generator 121-4 are 011, the inputs I(3) for the third priority generator 121-3 are 010 and so on. (This is with the buffer arbiter of FIG. 6, which grants priority based on the highest priority number. If the buffer arbiter grants priority based on the lowest priority number, then the initial starting values would be reversed so that inputs I for the fourth priority generator 121-4 are 000, the inputs I for the third priority generator 121-3 are 001 and so on.) The respective inputs I are loaded into the respective counter by enabling the load input L. After the initial values I are loaded into each counter, the count input CO of each counter is disabled. This fixes the outputs A at the programmed priorities. To change the priorities between the LANs, the inputs I are reprogrammed to new values, load L is enabled to pass the inputs I to the outputs A and disabled.

To provide for first-come first-serve priority, all of the counters 23 are loaded with the same initial starting values at inputs I. Thus, for example, all of the inputs I into all of the counters would be set at 000. Once these values are loaded into the counters, the count input CO of each counter is disabled to fix the outputs A."

As to the claimed invention of the present application as compared to Oman, the priority registers connected to the priority counters are defined by the different interrupts or channels such that each is associated to a counter that increases the priority in an uncorrelated manner with respect to the other interrupt channels. Clocks may be different. When a counter reaches an end count, it remains at a maximum value and waits as the interrupts are served. The event that increments the counter could be selected by the software as an operating system depending on the kind of algorithm that is to be implemented such that the interrupt is served within a fixed time period. The event is not necessarily a periodic signal (clock), but it can be a series of events coming from the external world, for example, the position of an internal combustion engine of a car that is accelerating or decelerating, as a non-limiting example.

Manber is directed to a first-come, first-serve arbitration protocol. The Examiner argues that Manber describes a function for inhibiting an "agent's" right to compete for arbitration after winning access to a resource until all other "agents" have been served, referring to column 3, lines 30-36 and 46-53. The Examiner considers this equivalent to canceling an interrupt and its priority from the pending and priority registers respectively after having been processed. Although Manber may suggest arbitrating control of a shared bus among different agents, it should be understood that each agent is provided with a total identity value including a less significant static portion and more significant dynamic portion. An increment line and request

line are wired to the agents. Manber is different because it teaches arbitrating for control of the bus in a single step arbitration based on total identity values of agents, and awarding control to the agent with the largest total identity value. Although the total identity value for each agent could be a priority value of a higher significance than a dynamic portion of each identity value, each agent increments its priority value so that it is greater than zero when it has a priority request for control of the bus and is included in the total identity value included in each arbitration.

This complicated function in Manber is more than simply canceling an interrupt and its priority from pending and priority registers after having been processed as seems to be suggested by the Examiner.

As to Norman, it uses the presence of a variable priority of packets that are to be sent by an input/output interface. Although the Examiner may argue that Norman teaches the incrementing of priority values of different periods that may be fixed or variable, it is functionally different and not as combinable as suggested. Norman suggests a particular case in which the actions to be carried out are pre-established, while in the claimed invention, the actions to be carried out depend on the corresponding interrupt request. In Norman, the priority may be increased only according to rules defined by pre-established functions such as a linear function, logarithmic function and similar functions without depending on external events. In the claimed invention of the instant application, however, the priority increment could be a periodic clock that increases interrupt priorities, but could also come from the external

world and not necessarily periodic as indicated above. The priority to be increased ensures that the corresponding interrupt is served while in Norman the packet could be deleted if it is too old.

Chou is specifically directed to an interrupt processing method and apparatus that is suited for an interrupt controller and shows a pending interrupt request operative with a priority compare tree and destination selection circuit. There are a plurality of destination processors. Each of the interrupt requests has at least one destination processor associated therewith for servicing the interrupt request. At least a portion of the interrupt requests are prioritized to identify a first priority interrupt request and second interrupt request. The appropriate destination processor is determined and, as a result of the determining step, the second interrupt request is masked such that the destination processor other than that selected for the first priority interrupt request is selected for the second interrupt request. First and second interrupt requests can be dispatched approximately simultaneously to different destination processors.

The claimed invention as presented in this Amendment does not suggest such destination processors with the circuit and function as set forth in Chou and is, at the least, much different and could typically be considered opposite in function.

Applicant contends that the present case is in condition for allowance and respectfully requests that the Examiner issue a Notice of Allowance and Issue Fee Due.

In re Patent Application of:
PEZZINI
Serial No. **10/717,177**
Filing Date: **November 19, 2003**

If the Examiner has any questions or suggestions for placing this case in condition for allowance, the undersigned attorney would appreciate a telephone call.

Respectfully submitted,

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Julie Lalan